RECEIVED
CENTRAL FAX CENTER

JAN 3 1 2006

ONS00555
10/813,501

FAX TRANSMITTAL FORM

TO: COMMISSIONER FOR PATENTS & TRADEMARKS
UNITED STATES PATENT & TRADEMARK OFFICE

FROM: LYDIA MCNAMARA
INTELLECTUAL PROPERTY DEPARTMENT
ON SEMICONDUCTOR
5005 EAST MCDOWELL ROAD
PHOENIX, AZ 85008

TEL. (602) 244-5603
FACSIMILE 602-244-3169

ONS00555
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DATE:	1/31/2006
IN RE APPLICATION OF:	ALAN R. BALL ET AL.
APPLN. NO.:	10/813501
FILED:	3/31/2004
FOR:	METHOD OF FORMING A SELF-GATED TRANSISTOR AND STRUCTURE THEREFOR
GROUP:	2816
EXAMINER:	QUAN TRA 571-272-1755

CERTIFICATE OF TRANSMITTAL VIA FACSIMILE

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO THE PATENT AND TRADEMARKOFFICE, ATTN EXAMINER QUAN TRA AT THE FAX NO. 571-273-8300

BY Lydia McNamara ON: 1/31/06
LYDIA MCNAMARA DATE

NUMBER OF PAGES INCLUDING THIS COVER PAGE: 16

RECEIVED
CENTRAL FAX CENTER
JAN 31 2006

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

FEE TRANSMITTAL

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Appliation Number	10/813501
Filing Date	March 31, 2004
First Named Inventor	Alan R. Ball et al.
Examiner Name	Quan Tra
Art Unit	2816
Attorney Docket No.	ONS00555

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account

Deposit Account Number: 501086
Deposit Account Name: Semiconductor Components Industries, LLC

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =	X	=
Independent Claims		-3** =	X	=
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	88	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	500.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) 1811 1.20(1) Certificate of Correction

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 500.00

SUBMITTED BY				(Complete *if applicable*)	
Name (Print/Type)	Robert F. Hightower	Registration No. (Attorney/Agent)	36,163	Telephone	(602) 244-5603
Signature	Robert F. Hightower			Date	1/31/2006

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

RECEIVED
CENTRAL FAX CENTER
JAN 3 1 2006

ONS00555

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DATE:	1/27/2006
IN RE APPLICATION OF:	ALAN R. BALL ET AL.
APPLN. NO.:	10/813501
FILED:	3/31/2004
FOR:	METHOD OF FORMING A SELF-GATED TRANSISTOR AND STRUCTURE THEREFOR
GROUP:	2816
EXAMINER:	QUAN TRA 571-272-1755

APPEAL BRIEF

I. REAL PARTY OF INTEREST

The real party of interest in this appeal is Semiconductor Components Industries, LLC (SCI), doing business as ON Semiconductor.

II. RELATED APPEALS AND INTERFERENCES

Applicants are not aware of any related appeals or interferences to this application.

III. STATUS OF THE CLAIMS

Claims 1-20 are in the proceeding.

Claims 1-20 are the claims on appeal.

A copy of the claims on appeal is provided in Section VIII, Claims Appendix.

Claims 1-20 are rejected.

02/01/2006 CNGUYEN 00000039 501086 10813501
01 FC:1402 500.00 DA

IV. STATUS OF THE AMENDMENTS

An Amendment was filed on September 26, 2005 and entered into the record.

A Response to a Final Rejection was filed on July 5, 2005 but was not entered into the record. The Response to the Final Rejection did not amend any of claims 1-20 but did add one new dependent claim which is not a part of this Appeal because the Response to the Final Rejection was not entered into the record.

An Advisory Action was issued on December 5, 2005 stating that applicants' Response to the Final Rejection would not be entered upon the filing of an appeal and that claims 1-20 would stand rejected.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The method of claim 1 calls for coupling a transistor operable to form a sense signal representative of a current through the self-gated transistor (as described on page 7, lines 17-19, and on page 8, lines 10-13); and,

configuring a first circuit of the self-gated transistor to disable the transistor substantially upon a positive current flow through the transistor (as described on page 8, lines 6-28) and to enable the transistor responsively to a negative current flow through the transistor (as described on page 7, line 11 through page 8, line 2).

As stated on page 8, lines 6-28, when the drain (node 27) of transistor 25 is pulled high (such as by transistor 16 being enabled) a positive current (30) flows through transistor 25. The positive current flow forms the sense signal (current 29) which causes comparator 42 to form a signal that disables transistor 31, thus, transistor 25. Conversely, (as stated on page 7, line 11 through page 8, line 2) when the drain (node 27) of transistor 25 is forced below the value of the voltage on the

source (node 28) of transistor 25, a negative current (negative value of current 30) flows that causes comparator 42 to enable transistor 31, thus, transistor 25.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Rejection of claims 1-20 under 35 U.S.C. §102(b) as being anticipated by Asada et al., USP 5,936,440 (hereinafter "Asada").

VII. ARGUMENTS

Arguments for allowability of Claims 1-7, Claims 8-11, and Claims 12-20 over Asada.

1. Claims 1-7.

Applicants' claim 1 includes, among other features, configuring a first circuit of the self-gated transistor to disable the transistor substantially upon a positive current flow through the transistor.

Applicants respectfully submit that Asada fails to disclose at least this element of claim 1.

The Advisory action states that "When the voltage at negative input of amplifier 840 is greater than Vr, the current flows through transistor 841 is a positive current; the output of 840 is low; the output of 501 is high; and the output of circuit 7 is low, thereby turns off transistor 841." Applicants respectfully disagree with this characterization of the operation of the circuit of Asada.

Applicants respectfully submit that Asada discloses in column 6, lines 16-34, the operation of the circuit of FIG. 4 and further states in line 45 that the function of comparator 840 is the same for both FIG. 4 and FIG. 5. In describing the reference voltage Vr, lines 21-22 of column 6 state that "The reference voltage Vr is negative and nearly ground potential". Asada further discloses in column 6, lines 23-34, that if the voltage

at node Vx lowers, a back-flow current flows through parasitic diode 100 and the voltage drop Vs becomes lower than the reference voltage Vr and the output of comparator 840 goes high which causes the enablement of transistor 10.

Applicants respectfully submit that as transistor 10 discharges field coil 32 the voltage Vx becomes less negative causing the current through resistor 801 and the corresponding voltage Vs at the negative input of comparator 840 to become less negative until voltage Vs becomes less negative than the negative reference voltage Vr. At that point, comparator 840 goes low to force gate 501 high and force circuit 7 low to disable transistors 10 and 841. Thus, transistors 10/841 are disabled by the current through resistor 801 being less negative to form voltage Vs less negative than reference voltage Vr. At the point where transistors 10/841 are disabled, the current flow through transistors 10/841 is still negative. Thus, transistors 10/841 are not disabled by a positive current flow through transistors 10/841 but are disabled by a less negative current. Consequently, this operation of the circuit in FIG. 5 of Asada does not disclose using a positive current to disable either of transistors 10 and 841.

Applicants further respectfully submit that in the circuit of FIG.s 4 or 5, there is no positive current flow through transistors 10/841. Once the less negative voltage from resistor 801 forces comparator 840 low to disable transistors 10/841, the low from comparator 840 prevents control signal Vc from affecting gate 501 which prevents control signal Vc from re-enabling transistor 10/841. The only way to re-enable transistors 10/841 is by voltage Vx again going negative (in response to signal Vc disabling transistor 9). As can be seen from FIG. 5, when signal Vc goes high to enable transistor 9, the low from comparator 840 continues to force gate 501 high and keep transistors 10/841 disabled. When control signal Vc goes low to disable transistor 9, transistor 10 remains disabled by comparator 840 and gate 501

until voltage Vx again goes negative to enable transistor 10. When transistors 10/841 are enabled by voltage Vx going negative (column 6, lines 23-31), the current through transistors 10/841 is negative. Thus, the Asada circuit of FIG. 5 (and FIG. 4) does not have a mode of operation that disables transistors 10/841 responsively to a positive current flow through transistor 10, but disables transistors 10/841 responsively to the voltage Vs (and the current through resistor 801) being less negative than reference Vr. Accordingly, applicants respectfully submit that claim 1 is not anticipated by Asada.

Also, Asada also does not anticipate claim 1 under the doctrine of inherency. For a claim element to be inherently disclosed by a reference, the allegedly inherent characteristic must necessarily flow from the teachings of the applied prior art (Ex parte Levy, 17 USPQ2d 1464). Applicants respectfully submit that it does not necessarily flow from the teachings of Asada that a positive current through transistor 10 (or 841) is used to disable transistor 10 because transistor 10 is disabled by a voltage that is less negative (resulting from a less negative current) than Vr.

Even if the structure of the Asada circuit 8b could somehow be construed to be similar to applicants, Asada does not disclose the method steps of claim 1. Consequently the method of claim 1 would at least be allowable as a new method of using an old structure under 35 U.S.C. section 100(b).

Claims 2-7 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

2. Claims 8-11.

Applicants' claim 8 includes, among other features, providing an MOS transistor ... wherein the sensing portion is operable to form a first sense signal representative of a first current through the main transistor portion;

configuring the self-gate transistor to detect the first sense signal and responsively disable the self-gated transistor;

configuring the self-gate transistor to conduct a second current ... wherein the second current flows in a direction opposite to the first current; and

configuring the self-gate transistor to detect the second sense signal and responsively enable the self-gated transistor.

Asada does not disclose a method of disabling the transistor for a current flow in one direction and enabling the transistor for a current flow in the opposite direction. As explained in the description of the traversal of the rejection of claim 1, applicants respectfully submit that Asada discloses disabling transistors 10/841 responsively to a voltage (resulting from a negative current) that is less negative than reference Vr and discloses enabling transistors 10/841 in response to a more negative current. Thus, as explained hereinbefore in the traversal of the rejection of claim 1, Asada discloses enabling and disabling transistors 10/841 in response to two different values of a negative current. Thus, applicants respectfully submit that transistors 10/841 are not disabled by a positive current flow through either of transistors 10/841 but are disabled by a current that becomes less negative to form a voltage that is less negative than the negative voltage Vr.

Also, Asada also does not anticipate claim 8 under the doctrine of inherency. For a claim element to be inherently disclosed by a reference, the allegedly inherent characteristic must necessarily flow from the teachings of the applied prior art (Ex parte Levy, 17 USPQ2d 1464). Applicants respectfully submit that it does not necessarily flow from the teachings of Asada that a positive current through transistor 10 (or 841) is used to disable transistor 10 because transistor 10 is disabled by a current that becomes less negative to form a voltage that is less negative than the negative voltage Vr.

Even if the structure of the Asada circuit 8b could somehow be construed to be similar to applicants, Asada does not disclose the method steps of claim 8. Consequently, the method of claim 8 would at least be allowable as a new method of using an old structure under 35 U.S.C. section 100(b).

Claims 9-11 depend from claim 8 and are believed to be allowable for at least the same reasons as claim 8.

3. Claims 12-20.

Applicants' claim 12 includes, among other features, a control circuit coupled to receive the sense signal and drive the first gate to enable the transistor responsively to a first polarity of the sense signal and to disable the transistor responsively to an opposite polarity of the sense signal.

Applicant's respectfully submit that Asada does not disclose a circuit that is coupled to disable the transistor responsively to an opposite polarity of the sense signal. As stated hereinbefore in the traversal of the rejection of claim 1, Asada discloses in column 6, lines 16-34 and line 45, enabling transistors 10/841 for a negative current flow through transistors 10/841 and disabling transistors 10/841 for a current that becomes less negative enough to form a voltage on the input of comparator 840 that is less negative than the negative value of reference voltage Vr. Thus, Asada discloses using a negative current for enabling transistors 10/841 and using a less negative current for disabling transistors 10/841. Both polarities of the current used by Asada are negative. Thus, applicants respectfully submit that transistors 10/841 are not disabled by a positive current flow through either of transistors 10/841.

Also, Asada also does not anticipate claim 12 under the doctrine of inherency. For a claim element to be inherently disclosed by a reference, the allegedly inherent characteristic must necessarily flow from the teachings of the applied prior art (Ex parte Levy, 17 USPQ2d 1464). Applicants respectfully submit

that it does not necessarily flow from the teachings of Asada that a positive current through transistor 10 (or 841) is used to disable transistor 10 because Asada discloses disabling transistor 10 a current that becomes less negative enough to form a voltage that is less negative than the negative voltage Vr.

Claims 13-20 depend from claim 12 and are believed to be allowable for at least the same reasons as claim 12.

Additionally, claim 19 includes, among other features, a voltage regulator coupled to provide an operating voltage to the comparator and coupled to a source of the self-gated transistor. Applicants respectfully submit that this element of claim 19 is not disclosed by Asada. The Final Office Action of July 5, 2005 states on page 5 that "is inherent for figure 5 to have a voltage regulator (circuit, not shown) coupled to provide an operating voltage to the comparator ... (the comparator must be powered in order to operate, the circuit, not shown, that powers the comparator is considered as a voltage regulator)."

It is well established that for a claim element to be inherent, it must necessarily flow from the teachings of the applied prior art. Applicants respectfully submit that it does not necessarily flow from the teachings of Asada that the circuit must have a voltage regulator coupled to provide an operating voltage. Applicants' argument is supported in FIG. 1 where Asada discloses that the power to operate circuit 4 is provided by battery 2, note the connection from battery 2 to terminal T3 of circuit 4. Thus, it is respectfully submitted that comparator 840 in FIG. 5 would also operate from battery 2 and that a separate voltage regulator is not required to provide the operating voltage to the comparator. Additionally, it is believed that Asada does not disclose any other source of operating power except battery 2. Accordingly, it is respectfully submitted that is not inherent that circuit 4 must have a voltage regulator to provide an operating voltage to the comparator. This is further supported by the fact that a

separate voltage regulator is not shown in FIG. 1. Accordingly, it is respectfully submitted that claim 19 is not anticipated by Asada.

Also, claim 20 includes, among other features, the self-gated transistor formed in a package having no greater than 4 leads. The Final Office Action of July 5, 2005 states on page 6 "figure 5 shows that the self-gated transistor formed in a package having no greater than four leads." Applicants respectfully submit that figure 5 is an illustration of a portion of FIG. 1, note column 6, lines 10-12, where Asada discloses that circuit 8 of FIG. 1 is replaced by a modified protection circuit 8a. FIG. 1 clearly shows that circuit 4, and correspondingly the circuit of FIG. 5, must have it least five terminals denoted as T1-T5. Accordingly, it is respectfully submitted that Asada cannot anticipate claim 20.

In view of the above, it is believed that Applicants' claims are allowable, and the Board of Appeals and Interferences is respectfully requested to reverse the Examiner.

If the Board of Appeals and Interferences rules that claims are allowable, applicants also respectfully request that the previous Response to the Final Action should also be entered into the record because the Response to the Final Action placed the claims in condition for allowance, thus, the refusal to enter the Response to the Final Action was improper.

Respectfully submitted,
Alan R. Ball et al., by

Robert F. Hightower

ON Semiconductor
Law Dept./MD A700
P.O. Box 62890
Phoenix, AZ 85082-2890

Customer #: 27255

Robert F. Hightower
Attorney for Applicant(s)

Reg. No. 36163
Tel. (602) 244-5603

VIII. CLAIMS APPENDIX

1. (Previously Presented) A method of forming a self-gated transistor comprising:

coupling a transistor operable to form a sense signal representative of a current through the self-gated transistor; and

configuring a first circuit of the self-gated transistor to disable the transistor substantially upon a positive current flow through the transistor and to enable the transistor responsively to a negative current flow through the transistor.

2. (Previously Presented) The method of claim 1 wherein coupling the transistor operable to form the sense signal representative of the current through the self-gated transistor includes forming the transistor having a main transistor portion and a sense transistor as a sensing portion including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form the sense signal representative of the current through the self-gated transistor.

3. (Original) The method of claim 2 wherein coupling the main transistor portion to the sensing portion includes coupling a drain of the sense transistor to a drain of the main transistor portion and to the drain of the self-gated transistor and also including coupling a gate of the sense transistor to a gate of the main transistor portion and to the gate of the self-gated transistor.

4. (Previously Presented) The method of claim 1 wherein configuring the first circuit of the self-gated transistor to disable the transistor substantially upon the positive current flow through the transistor and to enable the transistor responsively to the negative current flow through the transistor includes coupling a comparator to receive the sense signal wherein the sense signal is positive for the positive current flow and is negative for the negative current flow.

5. (Previously Presented) The method of claim 4 wherein coupling the comparator to receive the sense signal includes coupling a non-inverting input of the comparator to have a negative offset voltage.

6. (Previously Presented) The method of claim 4 wherein coupling the comparator to receive the sense signal includes coupling the comparator to responsively enable the self-gated transistor when the sense signal forms a voltage that is less than a voltage of a source of the self-gated transistor.

7. (Previously Presented) The method of claim 4 wherein coupling the comparator to receive the sense signal includes coupling one of a diode or a resistor between a source of a sense transistor and a source of the self-gated transistor.

8. (Previously Presented) A method of operating a self-gated transistor comprising:

providing an MOS transistor having a main transistor portion and a sensing portion including coupling the main transistor portion to the sensing portion wherein the sensing portion is operable to form a first sense signal representative of a first current through the main transistor portion;

configuring the self-gate transistor to detect the first sense signal and responsively disable the self-gated transistor;

configuring the self-gate transistor to conduct a second current through the sensing portion as a second sense signal wherein the second current flows in a direction opposite to the first current; and

configuring the self-gate transistor to detect the second sense signal and responsively enable the self-gated transistor.

9. (Previously Presented) The method of claim 8 wherein configuring the self-gate transistor to conduct the second current through the sensing portion as the second sense signal includes configuring the self-gate transistor to steer the second current to flow through a diode.

10. (Previously Presented) The method of claim 8 wherein configuring the self-gate transistor to conduct the second current through the sensing portion as the second sense signal includes configuring the self-gate transistor to steer the second sense current to flow through a resistor.

11. (Previously Presented) The method of claim 8 wherein configuring the self-gate transistor to detect the first sense signal and responsively disable the self-gated transistor includes coupling an input of a comparator to receive the first sense signal.

12. (Previously Presented) A self-gated transistor comprising:

a transistor having a main transistor portion and a sensing portion wherein the sensing portion is coupled to the main transistor portion to form a sense signal representative of a current through the self-gated transistor, the main transistor portion having a first gate; and

a control circuit coupled to receive the sense signal and drive the first gate to enable the transistor responsively to a first polarity of the sense signal and to disable the transistor responsively to an opposite polarity of the sense signal.

13. (Previously Presented) The self-gated transistor of claim 12 wherein the control circuit includes a comparator having an inverting input coupled to receive the sense signal.

14. (Original) The self-gated transistor of claim 13 wherein the comparator has a non-inverting input coupled to a source of the self-gated transistor.

15. (Original) The self-gated transistor of claim 14 wherein the non-inverting input of the comparator has a negative offset voltage.

16. (Cancelled)

17. (Original) The self-gated transistor of claim 12 further including the sensing portion having a source that is separate from a source of the main transistor portion and a protection circuit coupled to the source of the sensing portion.

18. (Original) The self-gated transistor of claim 12 wherein a source of the main transistor portion is coupled to a source of the self-gated transistor.

19. (Original) The self-gated transistor of claim 12 further including a voltage regulator coupled to provide an operating voltage to the comparator and coupled to a source of the self-gated transistor.

20. (Original) The self-gated transistor of claim 12 further including the self-gated transistor formed in a package having no greater than four leads.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to § 1.130, 1.131, 1.132.

X. RELATED PROCEEDINGS APPENDIX

The appellant is not aware of any related proceedings.